**Test plan:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ID | Description | Pre-condition | Expected input | Expected output | Actual output |
| H\_01 | NOT gate | For single input value only | 0 | 1 | 1 |
| H\_02\_L\_01 | AND gate | For two input values only | |  |  | | --- | --- | | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | |  | | --- | | 0 | | 0 | | 0 | | 1 | | |  | | --- | | 0 | | 0 | | 0 | | 1 | |
| H\_02\_L\_02 | AND gate | For three input values only | |  |  |  | | --- | --- | --- | | 0 | 0 | 0 | | 0 | 0 | 1 | | 0 | 1 | 0 | | 0 | 1 | 1 | | 1 | 0 | 0 | | 1 | 0 | 1 | | 1 | 1 | 0 | | 1 | 1 | 1 | | |  | | --- | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 1 | | |  | | --- | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 1 | |
| H\_03\_L\_01 | OR gate | For two input values only | |  |  | | --- | --- | | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | |  | | --- | | 0 | | 1 | | 1 | | 1 | | |  | | --- | | 0 | | 1 | | 1 | | 1 | |
| H\_03\_L\_02 | OR gate | For three input values only | |  |  |  | | --- | --- | --- | | 0 | 0 | 0 | | 0 | 0 | 1 | | 0 | 1 | 0 | | 0 | 1 | 1 | | 1 | 0 | 0 | | 1 | 0 | 1 | | 1 | 1 | 0 | | 1 | 1 | 1 | | |  | | --- | | 0 | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | |  | | --- | | 0 | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | |
| H\_04\_L\_01 | NAND gate | For two input values only | |  |  | | --- | --- | | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | |  | | --- | | 1 | | 1 | | 1 | | 0 | | |  | | --- | | 1 | | 1 | | 1 | | 0 | |
| H\_04\_L\_02 | NAND gate | For three input values only | |  |  |  | | --- | --- | --- | | 0 | 0 | 0 | | 0 | 0 | 1 | | 0 | 1 | 0 | | 0 | 1 | 1 | | 1 | 0 | 0 | | 1 | 0 | 1 | | 1 | 1 | 0 | | 1 | 1 | 1 | | |  | | --- | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | 0 | | |  | | --- | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | 0 | |
| H\_05\_L\_01 | NOR gate | For two input values only | |  |  | | --- | --- | | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | |  | | --- | | 1 | | 0 | | 0 | | 0 | | |  | | --- | | 1 | | 0 | | 0 | | 0 | |
| H\_05\_L\_02 | NOR gate | For three input values only | |  |  |  | | --- | --- | --- | | 0 | 0 | 0 | | 0 | 0 | 1 | | 0 | 1 | 0 | | 0 | 1 | 1 | | 1 | 0 | 0 | | 1 | 0 | 1 | | 1 | 1 | 0 | | 1 | 1 | 1 | | |  | | --- | | 1 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | |  | | --- | | 1 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | |
| H\_06\_L\_01 | XOR gate | For two input values only | |  |  | | --- | --- | | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | |  | | --- | | 0 | | 1 | | 1 | | 0 | | |  | | --- | | 0 | | 1 | | 1 | | 0 | |
| H\_06\_L\_02 | XOR gate | For three input values only | |  |  |  | | --- | --- | --- | | 0 | 0 | 0 | | 0 | 0 | 1 | | 0 | 1 | 0 | | 0 | 1 | 1 | | 1 | 0 | 0 | | 1 | 0 | 1 | | 1 | 1 | 0 | | 1 | 1 | 1 | | |  | | --- | | 0 | | 1 | | 1 | | 0 | | 1 | | 0 | | 0 | | 1 | | |  | | --- | | 0 | | 1 | | 1 | | 0 | | 1 | | 0 | | 0 | | 1 | |
| H\_07\_L\_01 | XNOR gate | For two input values only | |  |  | | --- | --- | | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | |  | | --- | | 1 | | 0 | | 0 | | 1 | | |  | | --- | | 1 | | 0 | | 0 | | 1 | |
| H\_07\_L\_02 | XNOR gate | For three input values only | |  |  |  | | --- | --- | --- | | 0 | 0 | 0 | | 0 | 0 | 1 | | 0 | 1 | 0 | | 0 | 1 | 1 | | 1 | 0 | 0 | | 1 | 0 | 1 | | 1 | 1 | 0 | | 1 | 1 | 1 | | |  | | --- | | 1 | | 0 | | 0 | | 1 | | 0 | | 1 | | 1 | | 0 | | |  | | --- | | 1 | | 0 | | 0 | | 1 | | 0 | | 1 | | 1 | | 0 | |